40 μA Micropower Instrumentation Amplifier with Zero Crossover Distortion

AD8236

FEATURES

Low power: 40 μA supply current (maximum)
Low input currents
- **1 pA input bias current**
- **0.5 pA input offset current**

High CMRR: 110 dB CMRR, G = 100
Space-saving MSOP
Zero input crossover distortion
Rail-to-rail input and output
Gain set with single resistor
Operates from 1.8 V to 5.5 V

APPLICATIONS

Medical instrumentation
Low-side current sense
Portable devices

CONNECTION DIAGRAM

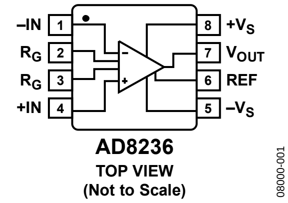


Figure 1.

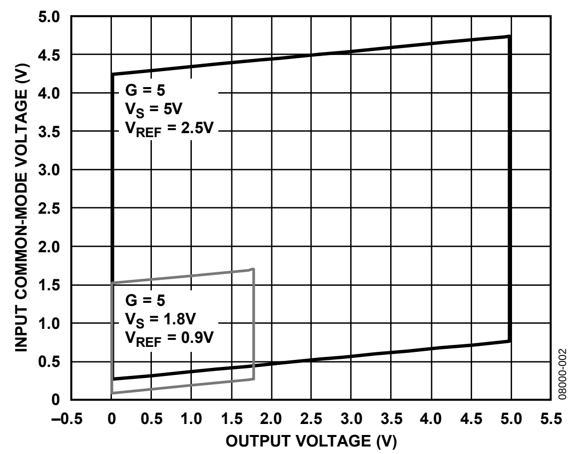


Figure 2. Wide Common-Mode Voltage Range vs. Output Voltage

GENERAL DESCRIPTION

The AD8236 is the lowest power instrumentation amplifier in the industry. It has rail-to-rail outputs and can operate on voltages as low as 1.8 V. Its 40 μA maximum supply current makes it an excellent choice in battery-powered applications.

The AD8236's high input impedance, low input bias current of 1 pA, high CMRR of 110 dB (G = 100), small size, and low power offer tremendous value. It has a wider common-mode voltage range than typical three-op-amp instrumentation amplifiers, making this a great solution for applications that operate on a single 1.8 V or 3 V supply. An innovative input stage allows for a wide rail-to-rail input voltage range without the crossover distortion common in other designs.

The AD8236 is available in an 8-lead MSOP and is specified over the industrial temperature range of −40°C to +125°C.

Table 1. Instrumentation Amplifiers by Category[1]

General Purpose	Zero Drift	Military Grade	Low Power	High Speed PGA
AD8220	AD8230	AD620	AD8236	AD8250
AD8221	AD8231	AD621	AD627	AD8251
AD8222	AD8290	AD624	AD623	AD8253
AD8228	AD8293G80	AD524	AD8223	
AD8295	AD8293G160	AD526	AD8226	
	AD8553			
	AD8556			
	AD8557			

[1] See www.analog.com/inamps for the latest instrumentation amplifiers.

Rev. 0

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 www.analog.com
Fax: 781.461.3113

TABLE OF CONTENTS

REVISION HISTORY

5/09—Revision 0: Initial Version

SPECIFICATIONS

$+V_S = 5$ V, $-V_S = 0$ V (GND), $V_{REF} = 2.5$ V, $T_A = 25°C$, G = 5, $R_L = 100$ kΩ to GND, unless otherwise noted.

Table 2.

Parameter	Test Conditions	Min	Typ	Max	Unit
COMMON-MODE REJECTION RATIO (CMRR)	$V_S = \pm 2.5$ V, $V_{REF} = 0$ V				
CMRR DC	$V_{CM} = -1.8$ V to +1.8 V				
G = 5		86	94		dB
G = 10		90	100		dB
G = 100		100	110		dB
G = 200		100	110		dB
NOISE					
Voltage Noise Spectral Density, RTI	f = 1 kHz, G = 5		76		nV/√Hz
RTI, 0.1 Hz to 10 Hz					
G = 5			4		μV p-p
G = 200			4		μV p-p
Current Noise			15		fA/√Hz
VOLTAGE OFFSET					
Input Offset, V_{OS}				3.5	mV
Average Temperature Coefficient (TC)	−40°C to +125°C		2.5		μV/°C
Offset RTI vs. Supply (PSR)	$V_S = 1.8$ V to 5 V				
G = 5		100	120		dB
G = 10		110	126		dB
G = 100		110	130		dB
G = 200		110	130		dB
INPUT CURRENT					
Input Bias Current			1	10	pA
Overtemperature	−40°C to +85°C			100	pA
	−40°C to +125°C			600	pA
Input Offset Current			0.5	5	pA
Overtemperature	−40°C to +85°C			50	pA
	−40°C to +125°C			130	pA
DYNAMIC RESPONSE					
Small Signal Bandwidth, −3 dB					
G = 5			23		kHz
G = 10			9		kHz
G = 100			0.8		kHz
G = 200			0.4		kHz
Settling Time 0.01%	$V_{OUT} = 4$ V step				
G = 5			444		μs
G = 10			456		μs
G = 100			992		μs
G = 200			1816		μs
Slew Rate					
G = 5 to 100			9		mV/μs

Parameter	Test Conditions	Min	Typ	Max	Unit
GAIN					
Gain Range	$G = 5 + 420\ k\Omega/R_G$	5		200[1]	V/V
Gain Error	$V_S = \pm2.5\ V$, $V_{REF} = 0\ V$, $V_{OUT} = -2\ V$ to $+2\ V$				
G = 5			0.005	0.05	%
G = 10			0.03	0.2	%
G = 100			0.06	0.2	%
G = 200			0.15	0.3	%
Nonlinearity	$R_L = 10\ k\Omega$ or $100\ k\Omega$				
G = 5			2	10	ppm
G = 10			1.2	10	ppm
G = 100			0.5	10	ppm
G = 200			0.5	10	ppm
Gain vs. Temperature	−40°C to +125°C				
G = 5			0.25	1	ppm/°C
G > 10				−50	ppm/°C
INPUT					
Differential Impedance			440‖1.6		GΩ‖pF
Common-Mode Impedance			110‖6.2		GΩ‖pF
Input Voltage Range	−40°C to +125°C	0		$+V_S$	V
OUTPUT					
Output Voltage High, V_{OH}	$R_L = 100\ k\Omega$	4.98	4.99		V
	−40°C to +125°C	4.98			V
	$R_L = 10\ k\Omega$	4.9	4.95		V
	−40°C to +125°C	4.9			V
Output Voltage Low, V_{OL}	$R_L = 100\ k\Omega$		2	5	mV
	−40°C to +125°C			5	mV
	$R_L = 10\ k\Omega$		10	25	mV
	−40°C to +125°C			30	mV
Short-Circuit Limit, I_{SC}			±55		mA
REFERENCE INPUT					
R_{IN}	−IN, +IN = 0 V		210		kΩ
I_{IN}			20		nA
Voltage Range		$-V_S$		$+V_S$	V
Gain to Output			1		V/V
POWER SUPPLY					
Operating Range		1.8		5.5	V
Quiescent Current			30	40	μA
Overtemperature	−40°C to +125°C			50	μA
TEMPERATURE RANGE					
For Specified Performance		−40		+125	°C

[1] Although the specifications of the AD8236 list only low to midrange gains, gains can be set beyond 200.

$+V_S$ = 1.8 V, $-V_S$ = 0 V (GND), V_{REF} = 0.9 V, T_A = 25°C, G = 5, R_L = 100 kΩ to GND, unless otherwise noted.

Table 3.

Parameter	Test Conditions	Min	Typ	Max	Unit
COMMON-MODE REJECTION RATIO (CMRR)	V_S = ±0.9 V, V_{REF} = 0 V				
CMRR DC	V_{CM} = −0.6 V to +0.6 V				
G = 5		86	94		dB
G = 10		90	100		dB
G = 100		100	110		dB
G = 200		100	110		dB
NOISE					
Voltage Noise Spectral Density, RTI	f = 1 kHz, G = 5		76		nV/√Hz
RTI, 0.1 Hz to 10 Hz					
G = 5			4		μV p-p
G = 200			4		μV p-p
Current Noise			15		fA/√Hz
VOLTAGE OFFSET					
Input Offset, V_{OS}				3.5	mV
Average Temperature Coefficient (TC)	−40°C to +125°C		2.5		μV/°C
Offset RTI vs. Supply (PSR)	V_S = 1.8 V to 5 V				
G = 5		100	120		dB
G = 10		110	126		dB
G = 100		110	130		dB
G = 200		110	130		dB
INPUT CURRENT					
Input Bias Current			1	10	pA
Overtemperature	−40°C to +85°C			100	pA
	−40°C to +125°C			600	pA
Input Offset Current			0.5	5	pA
Overtemperature	−40°C to +85°C			50	pA
	−40°C to +125°C			130	pA
DYNAMIC RESPONSE					
Small Signal Bandwidth, −3 dB					
G = 5			23		kHz
G = 10			9		kHz
G = 100			0.8		kHz
G = 200			0.4		kHz
Settling Time 0.01%	V_{OUT} = 1.4 V step				
G = 5			143		μs
G = 10			178		μs
G = 100			1000		μs
G = 200			1864		μs
Slew Rate					
G = 5 to 100			11		mV/μs
GAIN					
Gain Range	G = 5 + 420 kΩ/R_G	5		200[1]	V/V
Gain Error	V_S = ±0.9 V, V_{REF} = 0 V, V_{OUT} = −0.6 V to +0.6 V				
G = 5			0.005	0.05	%
G = 10			0.03	0.2	%
G = 100			0.06	0.2	%
G = 200			0.15	0.3	%

Parameter	Test Conditions	Min	Typ	Max	Unit
Nonlinearity	R_L = 10 kΩ or 100 kΩ				
G = 5			1	10	ppm
G = 10			1	10	ppm
G = 100			0.5	10	ppm
G = 200			0.4	10	ppm
Gain vs. Temperature	−40°C to +125°C				
G = 5			0.25	1	ppm/°C
G > 10				−50	ppm/°C
INPUT					
Differential Impedance			440‖1.6		GΩ‖pF
Common-Mode Impedance			110‖6.2		GΩ‖pF
Input Voltage Range	−40°C to +125°C	0		$+V_S$	V
OUTPUT					
Output Voltage High, V_{OH}	R_L = 100 kΩ	1.78	1.79		V
	−40°C to +125°C	1.78			V
	R_L = 10 kΩ	1.65	1.75		V
	−40°C to +125°C	1.65			V
Output Voltage Low, V_{OL}	R_L = 100 kΩ		2	5	mV
	−40°C to +125°C			5	mV
	R_L = 10 kΩ		12	25	mV
	−40°C to +125°C			25	mV
Short-Circuit Limit, I_{SC}			±6		mA
REFERENCE INPUT					
R_{IN}	−IN, +IN = 0 V		210		kΩ
I_{IN}			20		nA
Voltage Range		$-V_S$		$+V_S$	V
Gain to Output			1		V/V
POWER SUPPLY					
Operating Range		1.8		5.5	V
Quiescent Current			33	40	µA
Overtemperature	−40°C to +125°C			50	µA
TEMPERATURE RANGE					
For Specified Performance		−40		+125	°C

[1] Although the specifications of the AD8236 list only low to midrange gains, gains can be set beyond 200.

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Supply Voltage	6 V
Power Dissipation	See Figure 3
Output Short-Circuit Current	55 mA
Input Voltage (Common Mode)	$\pm V_S$
Differential Input Voltage	$\pm V_S$
Storage Temperature Range	−65°C to +125°C
Operating Temperature Range	−40°C to +125°C
Lead Temperature (Soldering, 10 sec)	300°C
Junction Temperature	140°C
θ_{JA} (4-Layer JEDEC Standard Board)	
8-Lead MSOP	135°C/W
Package Glass Transition Temperature	
8-Lead MSOP	140°C
ESD	
Human Body Model	2 kV
Charge Device Model	1 kV
Machine Model	200 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

MAXIMUM POWER DISSIPATION

The maximum safe power dissipation in the package of the AD8236 is limited by the associated rise in junction temperature (T_J) on the die. The plastic encapsulating the die locally reaches the junction temperature. At approximately 140°C, which is the glass transition temperature, the plastic changes its properties. Even temporarily exceeding this temperature limit may change the stresses that the package exerts on the die, permanently shifting the parametric performance of the AD8236.

The still-air thermal properties of the package and PCB (θ_{JA}), the ambient temperature (T_A), and the total power dissipated in the package (P_D) determine the junction temperature of the die. The junction temperature is calculated as

$$T_J = T_A + (P_D \times \theta_{JA})$$

The power dissipated in the package (P_D) is the sum of the quiescent power dissipation and the power dissipated in the package due to the load drive for all outputs. The quiescent power is the voltage between the supply pins (V_S) times the quiescent current (I_S). Assuming the load (R_L) is referenced to midsupply, the total drive power is $V_S/2 \times I_{OUT}$, some of which is dissipated in the package and some in the load ($V_{OUT} \times I_{OUT}$).

The difference between the total drive power and the load power is the drive power dissipated in the package.

$$P_D = \text{Quiescent Power} + (\text{Total Drive Power} - \text{Load Power})$$

$$P_D = (V_S \times I_S) + \left(\frac{V_S}{2} \times \frac{V_{OUT}}{R_L}\right) - \frac{V_{OUT}^2}{R_L}$$

RMS output voltages should be considered. If R_L is referenced to $-V_S$, as in single-supply operation, the total drive power is $V_S \times I_{OUT}$. If the rms signal levels are indeterminate, consider the worst case, when $V_{OUT} = V_S/4$ for R_L to midsupply

$$P_D = (V_S \times I_S) + \frac{(V_S/4)^2}{R_L}$$

In single-supply operation with R_L referenced to $-V_S$, worst case is $V_{OUT} = V_S/2$.

Airflow increases heat dissipation, effectively reducing θ_{JA}. In addition, more metal directly in contact with the package leads from metal traces, through holes, ground, and power planes reduces the θ_{JA}.

Figure 3 shows the maximum safe power dissipation in the package vs. the ambient temperature for the 8-lead MSOP on a 4-layer JEDEC standard board. θ_{JA} values are approximations.

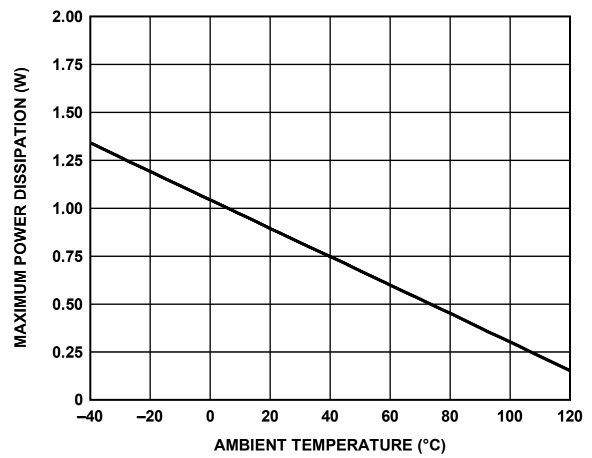
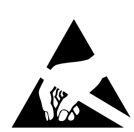


Figure 3. Maximum Power Dissipation vs. Ambient Temperature

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

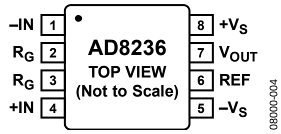


Figure 4. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	−IN	Negative Input Terminal (True Differential Input)
2, 3	R_G	Gain Setting Terminals (Place Resistor Across the R_G Pins)
4	+IN	Positive Input Terminal (True Differential Input)
5	$-V_S$	Negative Power Supply Terminal
6	REF	Reference Voltage Terminal (Drive This Terminal with a Low Impedance Voltage Source to Level-Shift the Output)
7	V_{OUT}	Output Terminal
8	$+V_S$	Positive Power Supply Terminal

TYPICAL PERFORMANCE CHARACTERISTICS

G = 5, $+V_S$ = 5 V, V_{REF} = 2.5 V, R_L = 100 kΩ tied to GND, T_A = 25°C, unless otherwise noted.

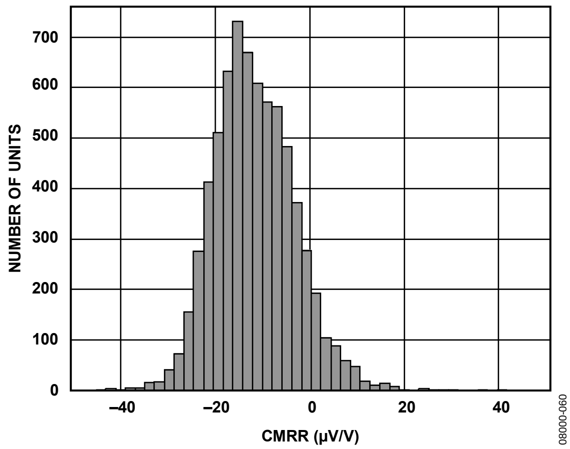


Figure 5. Typical Distribution of CMRR, G = 5

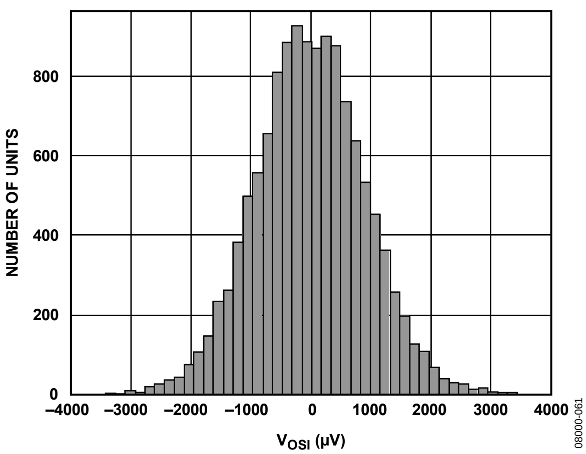


Figure 6. Typical Distribution of Input Offset Voltage

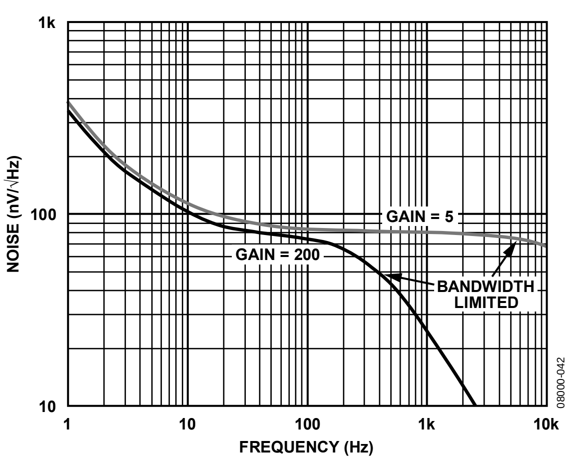


Figure 7. Voltage Noise Spectral Density vs. Frequency

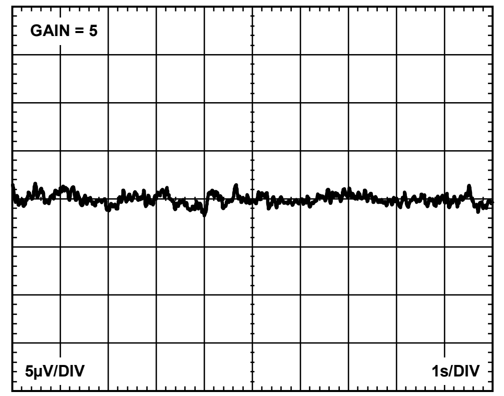


Figure 8. 0.1 Hz to 10 Hz RTI Voltage Noise

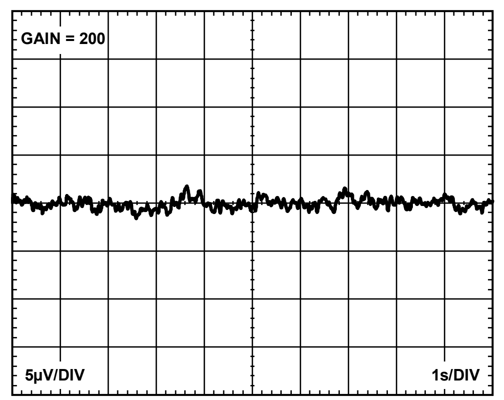


Figure 9. 0.1 Hz to 10 Hz RTI Voltage Noise

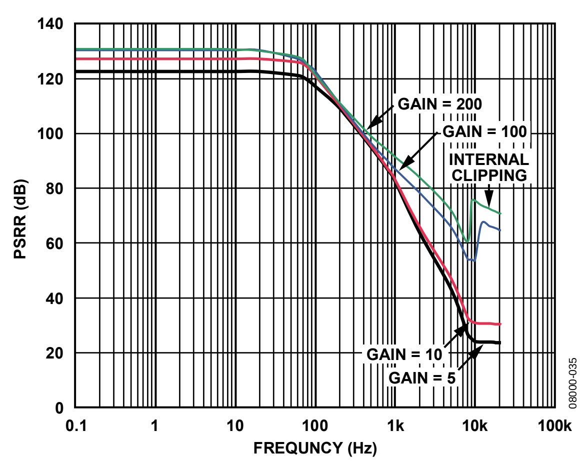


Figure 10. Positive PSRR vs. Frequency, RTI, V_S = ±0.9 V, ±2.5 V, V_{REF} = 0 V

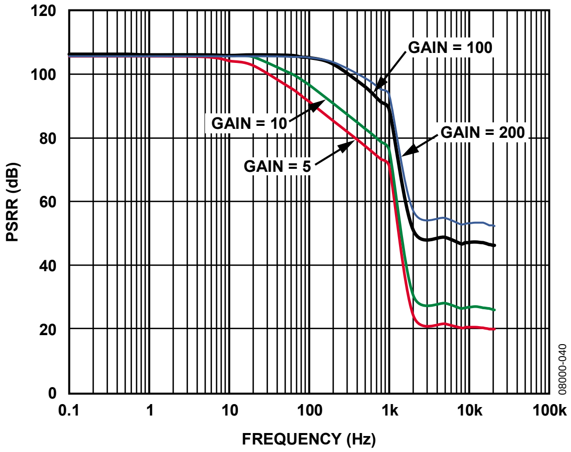


Figure 11. Negative PSRR vs. Frequency, RTI, $V_S = \pm0.9$ V, ±2.5 V, $V_{REF} = 0$ V

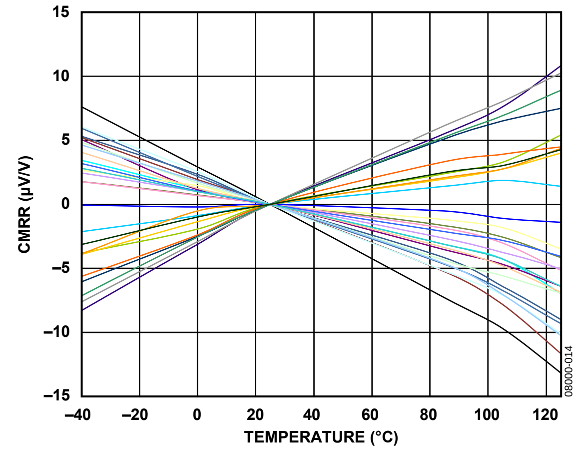


Figure 14. Change in CMRR vs. Temperature, G = 5, Normalized at 25°C

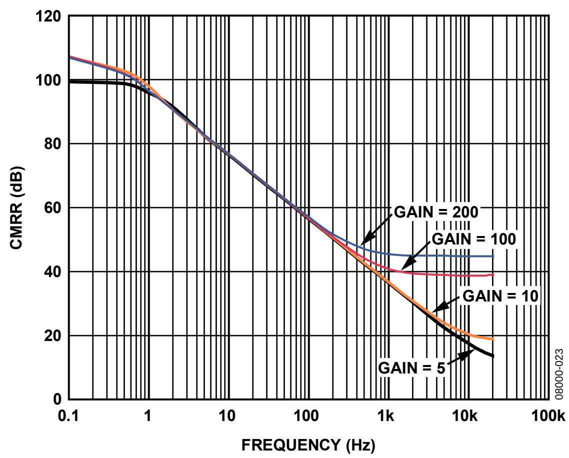


Figure 12. CMRR vs. Frequency, RTI

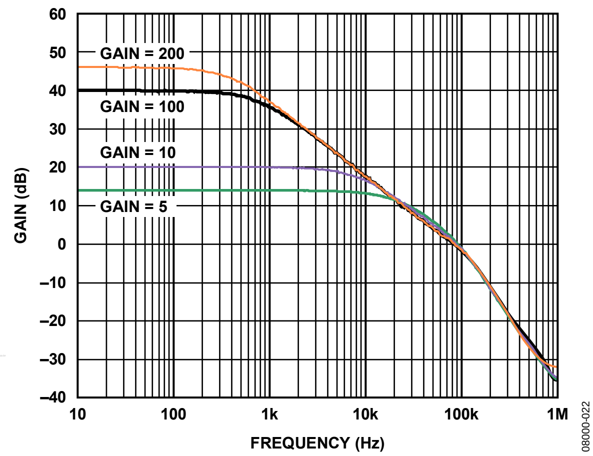


Figure 15. Gain vs. Frequency, $V_S = 1.8$ V, 5 V

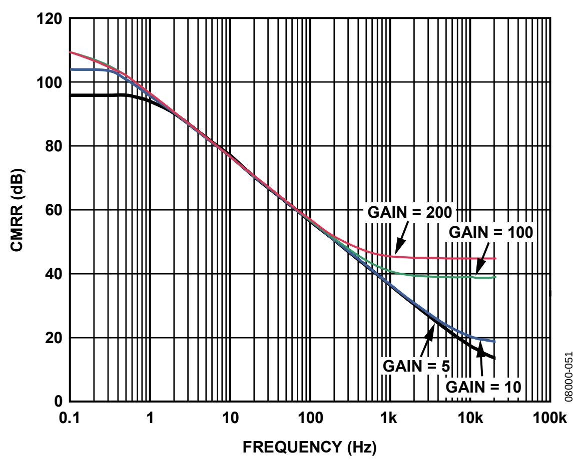


Figure 13. CMRR vs. Frequency, 1 kΩ Source Imbalance, RTI

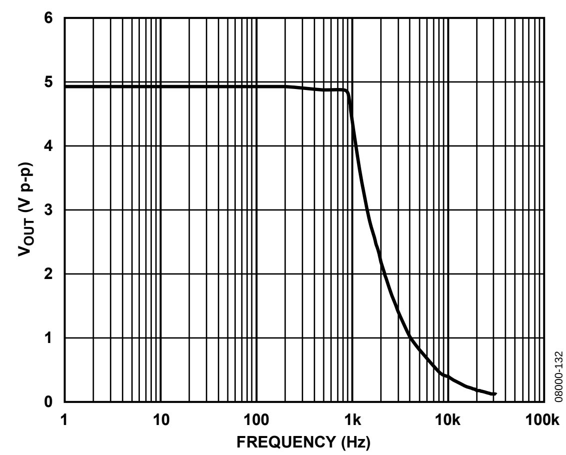


Figure 16. Maximum Output Voltage vs. Frequency

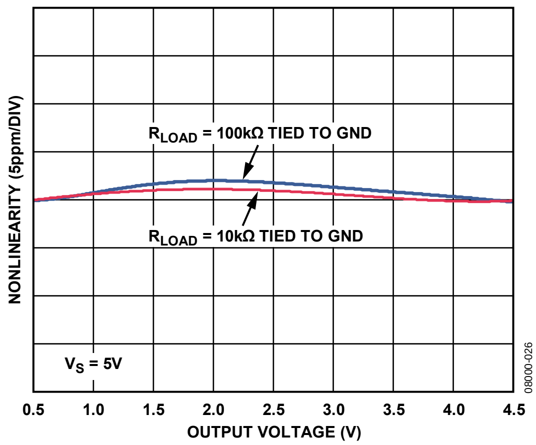


Figure 17. Gain Nonlinearity, G = 5

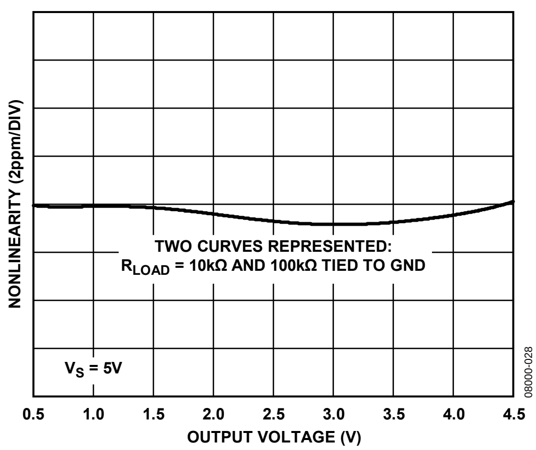


Figure 18. Gain Nonlinearity, G = 10

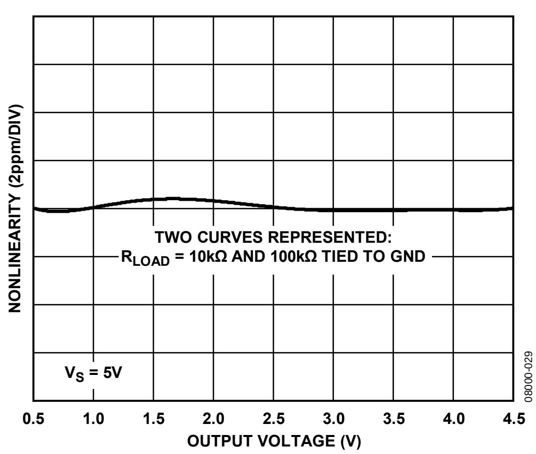


Figure 19. Gain Nonlinearity, G = 200

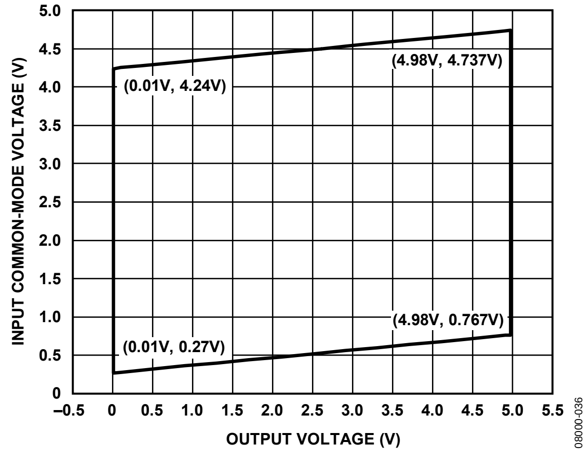


Figure 20. Input Common-Mode Voltage Range vs. Output Voltage, G = 5, V_S = 5 V, V_{REF} = 2.5 V

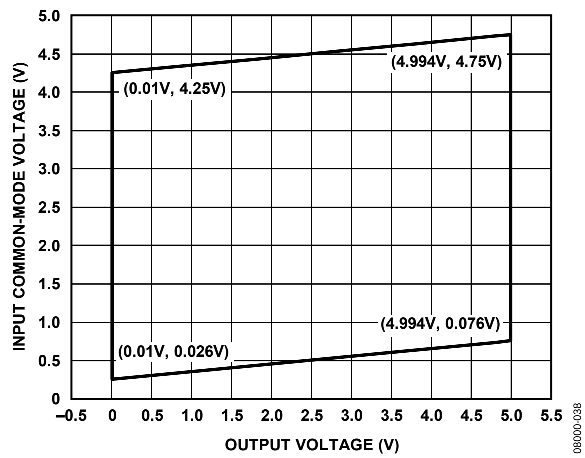


Figure 21. Input Common-Mode Voltage Range vs. Output Voltage, G = 200, V_S = 5 V, V_{REF} = 2.5 V

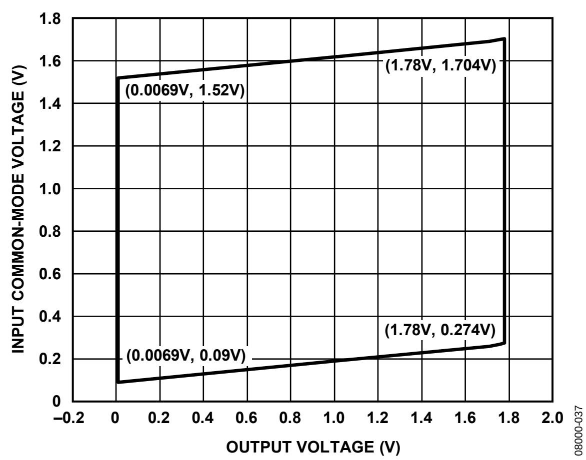


Figure 22. Input Common-Mode Voltage Range vs. Output Voltage, G = 5, V_S = 1.8 V, V_{REF} = 0.9 V

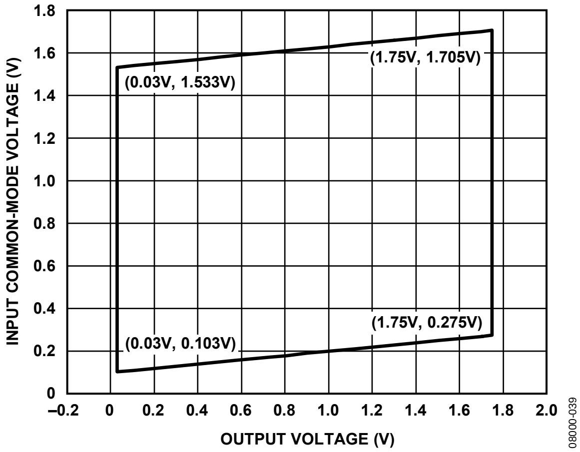


Figure 23. Input Common-Mode Voltage Range vs. Output Voltage, G = 200, V_S = 1.8 V, V_{REF} = 0.9 V

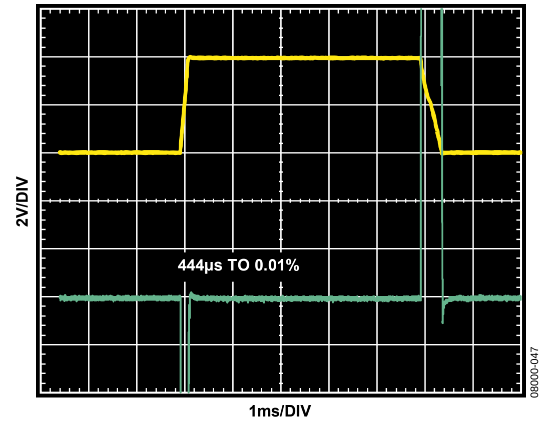


Figure 26. Large Signal Pulse Response and Settling Time, V_S = ±2.5 V, V_{REF} = 0 V, R_L = 10 kΩ to V_{REF}

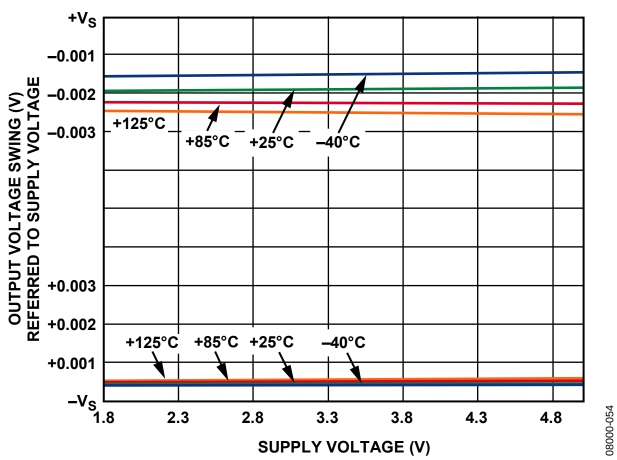


Figure 24. Output Voltage Swing vs. Supply Voltage, V_S = ±0.9 V, ±2.5 V, V_{REF} = 0 V, R_L = 100 kΩ Tied to $-V_S$

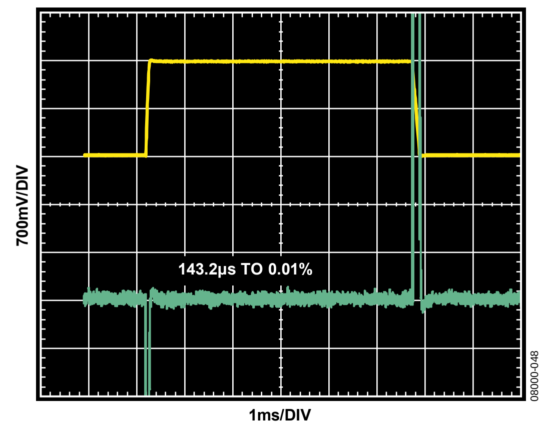


Figure 27. Large Signal Pulse Response and Settling Time, V_S = ±0.9 V, V_{REF} = 0 V, R_L = 10 kΩ to V_{REF}

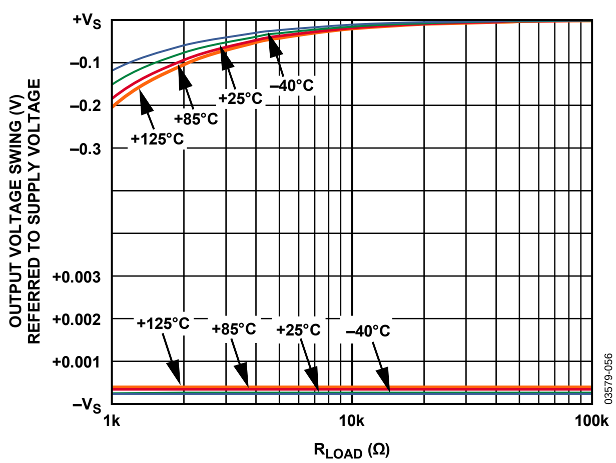


Figure 25. Output Voltage Swing vs. Load Resistance, V_S = ±0.9 V, ±2.5 V, V_{REF} = 0 V, R_L = 100 kΩ Tied to $-V_S$

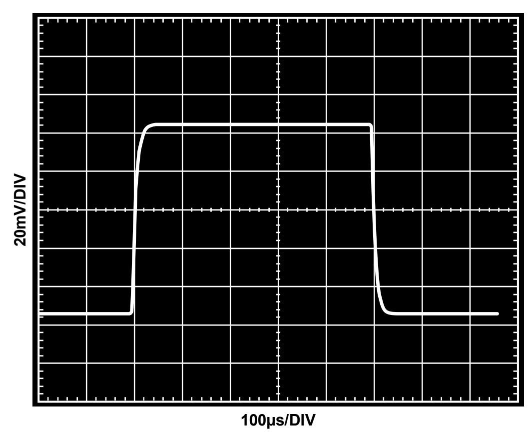


Figure 28. Small Signal Pulse Response, G = 5, V_S = ±2.5 V, V_{REF} = 0 V, R_L = 100 kΩ to V_{REF}, C_L = 100 pF

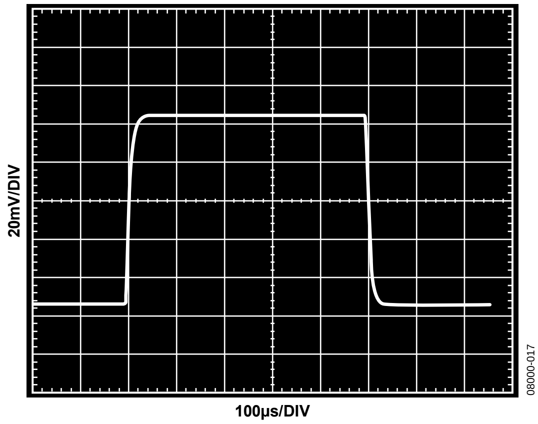


Figure 29. Small Signal Pulse Response, G = 5, C_L = 100 pF, V_S = ±0.9 V, V_{REF} = 0 V, R_L = 100 kΩ to V_{REF}

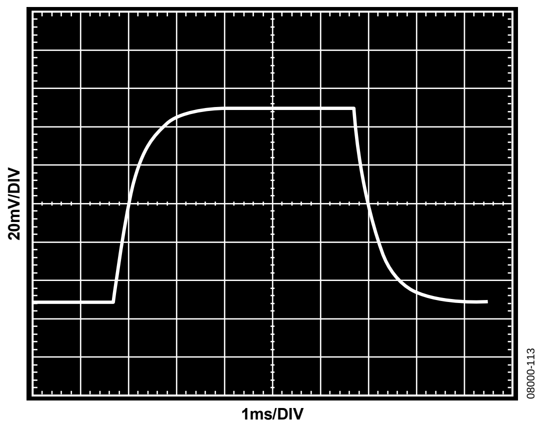


Figure 30. Small Signal Pulse Response, G = 200, C_L = 100 pF, V_S = 2.5 V, V_{REF} = 0 V, R_L = 100 kΩ to V_{REF}

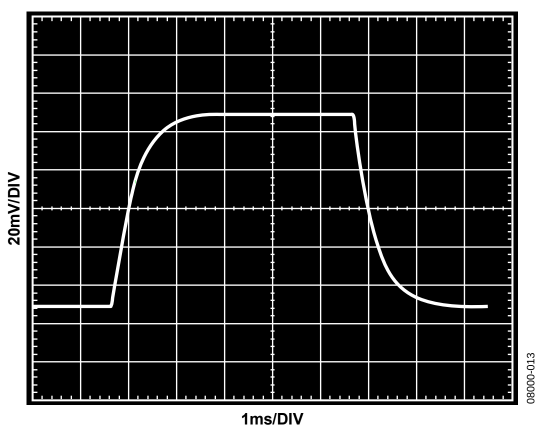


Figure 31. Small Signal Pulse Response, G = 200, C_L = 100 pF, V_S = 0.9 V, V_{REF} = 0 V, R_L = 100 kΩ to V_{REF}

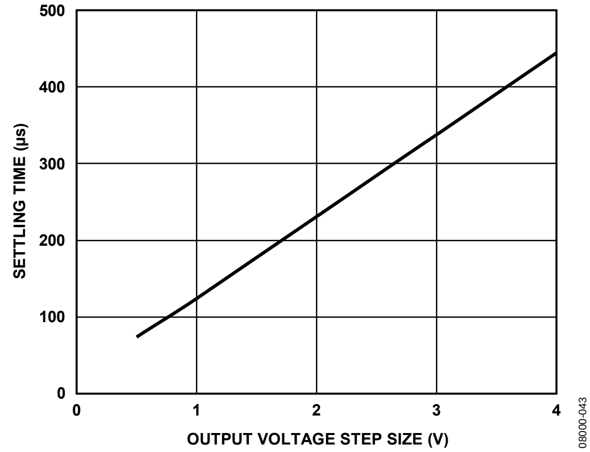


Figure 32. Settling Time vs. Output Voltage Step Size, V_S = ±2.5 V, V_{REF} = 0 V, R_L = 10 kΩ Tied to V_{REF}

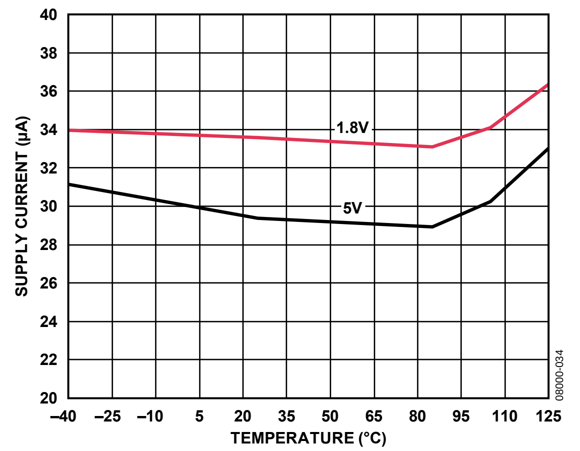


Figure 33. Total Supply Current vs. Temperature

THEORY OF OPERATION

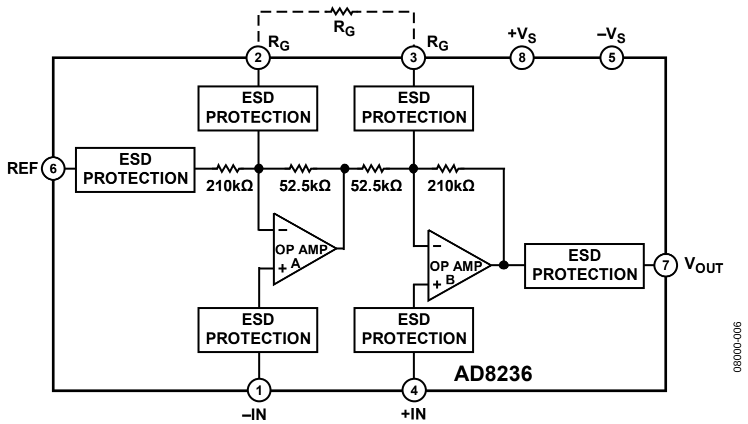


Figure 34. Simplified Schematic

The AD8236 is a monolithic, 2-op-amp instrumentation amplifier. It was designed for low power, portable applications where size and low quiescent current are paramount. For example, it has a rail-to-rail input and output stage to offer more dynamic range when operating on low voltage batteries. Unlike traditional rail-to-rail input amplifiers that use a complementary differential pair stage and suffer from nonlinearity, the AD8236 uses a novel architecture to internally boost the supply rail, allowing the amplifier to operate rail to rail yet still deliver a low 0.5 ppm of nonlinearity. In addition, the 2-op-amp instrumentation amplifier architecture offers a wide operational common-mode voltage range. Additional information is provided in the Common-Mode Input Voltage Range section. Precision, laser-trimmed resistors provide the AD8236 with a high CMRR of 86 dB (minimum) at G = 5 and gain accuracy of 0.05% (maximum).

BASIC OPERATION

The AD8236 amplifies the difference between its positive input (+IN) and its negative input (–IN). The REF pin allows the user to level-shift the output signal. This is convenient when interfacing to a filter or analog-to-digital converter (ADC). The basic setup is shown in Figure 35. Figure 37 shows an example configuration for operating the AD8236 with dual supplies. The equation for the AD8236 is as follows:

$$V_{OUT} = G \times (VINP - VINM) + VREF$$

If no gain setting resistor is installed, the default gain, G, is 5. The Gain Selection section describes how to program the gain, G.

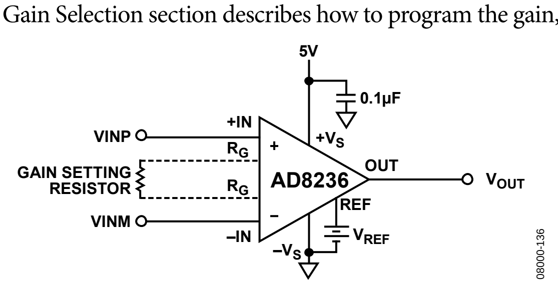


Figure 35. Basic Setup

GAIN SELECTION

Placing a resistor across the R_G terminals sets the gain of the AD8236, which can be calculated by referring to Table 6 or by using the gain equation

$$R_G = \frac{420\ \text{k}\Omega}{G - 5}$$

Table 6. Gains Achieved Using 1% Resistors

1% Standard Table Value of R_G (Ω)	Calculated Gain
422 k	6.0
210 k	7.0
140 k	8.0
105 k	9.0
84.5 k	10.0
28 k	20.0
9.31 k	50.1
4.42 k	100.0
2.15 k	200.3

The AD8236 defaults to G = 5 when no gain resistor is used. Gain accuracy is determined by the absolute tolerance of R_G. The TC of the external gain resistor increases the gain drift of the instrumentation amplifier. Gain error and gain drift are at a minimum when the gain resistor is not used.

LAYOUT

Careful board layout maximizes system performance. In applications that need to take advantage of the low input bias current of the AD8236, avoid placing metal under the input path to minimize leakage current.

Grounding

The output voltage of the AD8236 is developed with respect to the potential on the reference terminal, REF. To ensure the most accurate output, the trace from the REF pin should either be connected to the AD8236 local ground (see Figure 37) or connected to a voltage that is referenced to the AD8236 local ground (Figure 35).

REFERENCE TERMINAL

The reference terminal, REF, is at one end of a 210 kΩ resistor (see Figure 34). The output of the instrumentation amplifier is referenced to the voltage on the REF terminal; this is useful when the output signal needs to be offset to voltages other than common. For example, a voltage source can be tied to the REF pin to level-shift the output so that the AD8236 can interface with an ADC. The allowable reference voltage range is a function of the gain, common-mode input, and supply voltages. The REF pin should not exceed either $+V_S$ or $-V_S$ by more than 0.5 V.

For best performance, especially in cases where the output is not measured with respect to the REF terminal, source impedance to the REF terminal should be kept low because parasitic resistance can adversely affect CMRR and gain accuracy. Figure 36 demonstrates how an op amp is configured to provide a low source impedance to the REF terminal when a midscale reference voltage is desired.

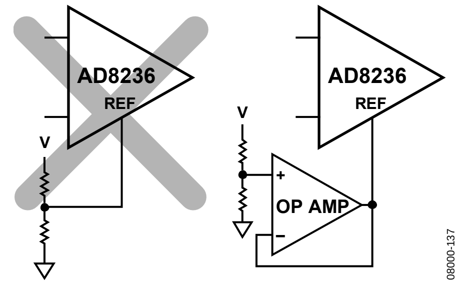


Figure 36. Driving the REF Pin

POWER SUPPLY REGULATION AND BYPASSING

The AD8236 has high power supply rejection ration (PSRR). However, for optimal performance, a stable dc voltage should be used to power the instrumentation amplifier. Noise on the supply pins can adversely affect performance. As in all linear circuits, bypass capacitors must be used to decouple the amplifier.

A 0.1 µF capacitor should be placed close to each supply pin. A 10 µF tantalum capacitor can be used further away from the part (see Figure 37). In most cases, it can be shared by other precision integrated circuits.

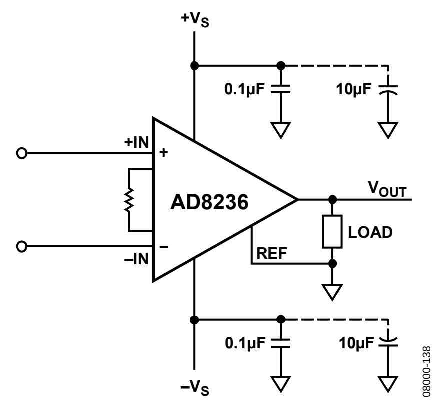


Figure 37. Supply Decoupling, REF, and Output Referred to Ground

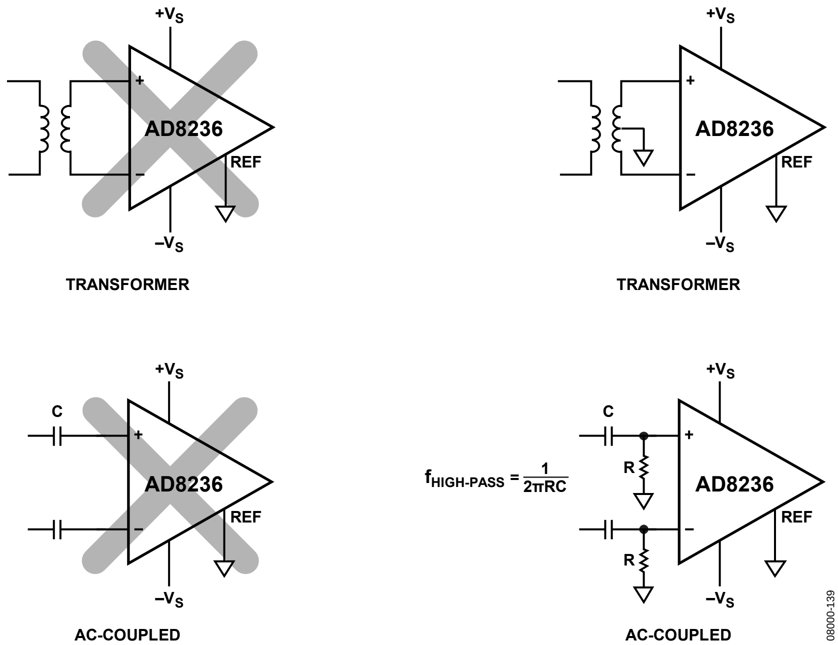


Figure 38. Creating an I_{BIAS} Path

INPUT BIAS CURRENT RETURN PATH

The AD8236 input bias current is extremely small at less than 10 pA. Nonetheless, the input bias current must have a return path to common. When the source, such as a transformer, cannot provide a return current path, one should be created (see Figure 38).

INPUT PROTECTION

All terminals of the AD8236 are protected against ESD. In addition, the input structure allows for dc overload conditions a diode drop above the positive supply and a diode drop below the negative supply. Voltages beyond a diode drop of the supplies cause the ESD diodes to conduct and enable current to flow through the diode. Therefore, an external resistor should be used in series with each of the inputs to limit current for voltages above $+V_S$. In either scenario, the AD8236 safely handles a continuous 6 mA current at room temperature.

For applications where the AD8236 encounters extreme overload voltages, as in cardiac defibrillators, external series resistors and low leakage diode clamps, such as BAV199Ls, FJH1100s, or SP720s, should be used.

RF INTERFERENCE

RF rectification is often a problem in applications where there are large RF signals. The problem appears as a small dc offset voltage. The AD8236, by its nature, has a 3.1 pF gate capacitance, C_G, at each input. Matched series resistors form a natural low-pass filter that reduces rectification at high frequency (see Figure 39). The relationship between external, matched series resistors and the internal gate capacitance is expressed as

$$FilterFreq_{DIFF} = \frac{1}{2\pi RC_G}$$

$$FilterFreq_{CM} = \frac{1}{2\pi RC_G}$$

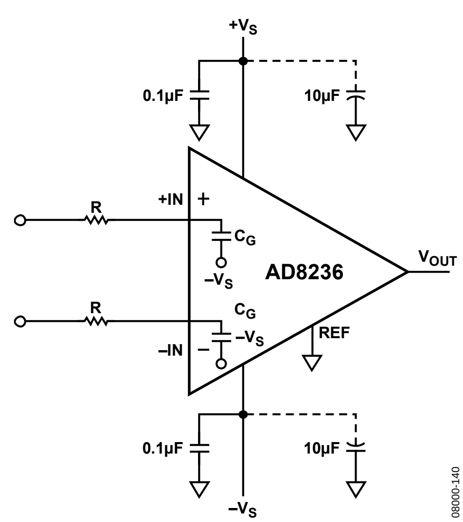


Figure 39. RFI Filtering Without External Capacitors

To eliminate high frequency common-mode signals while using smaller source resistors, a low-pass RC network can be placed at the input of the instrumentation amplifier (see Figure 40). The filter limits the input signal bandwidth according to the following relationship:

$$FilterFreq_{DIFF} = \frac{1}{2\pi R(2\,C_D + C_C + C_G)}$$

$$FilterFreq_{CM} = \frac{1}{2\pi R(C_C + C_G)}$$

Mismatched C_C capacitors result in mismatched low-pass filters. The imbalance causes the AD8236 to treat what would have been a common-mode signal as a differential signal. To reduce the effect of mismatched external C_C capacitors, select a value of C_D greater than 10 times C_C. This sets the differential filter frequency lower than the common-mode frequency.

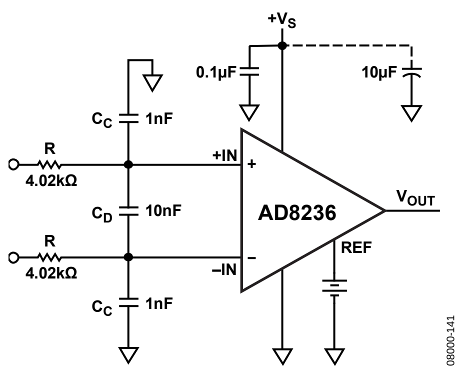


Figure 40. RFI Suppression

COMMON-MODE INPUT VOLTAGE RANGE

The common-mode input voltage range is a function of the input voltages, reference voltage, supplies, and the output of Internal Op Amp A. Figure 34 shows the internal nodes of the AD8236. Figure 20 to Figure 23 show the common-mode voltage ranges for typical supply voltages and gains.

If the supply voltages and reference voltage is not represented in Figure 20 to Figure 23, the following methodology can be used to calculate the acceptable common-mode voltage range:

1. Adhere to the input, output, and reference voltage ranges shown in Table 2 and Table 3**.**
2. Calculate the output of the internal op amp, A. The following equation calculates this output:

$$A = \frac{5}{4}\left(V_{CM} - \frac{V_{DIFF}}{2}\right) - \frac{52.5\text{ k}\Omega}{\text{R}_\text{G}} V_{DIFF} - \frac{V_{REF}}{4}$$

   where:
   V_{DIFF} is defined as the difference in input voltages,
   V_{DIFF} = VINP − VINM.
   V_{CM} is defined as the common mode voltage,
   V_{CM} = (VINP + VINM)/2.

   If no gain setting resistor, R_G, is installed, set R_G to infinity.

3. Keep A within 10 mV of either supply rail. This is valid over the −40°C to +125°C temperature range.

   $-V_S + 10\text{ mV} < A < +V_S - 10\text{ mV}$

APPLICATIONS INFORMATION

AC-COUPLED INSTRUMENTATION AMPLIFIER

An integrator can be tied to the AD8236 in feedback to create a high-pass filter as shown in Figure 41. This circuit can be used to reject dc voltages and offsets. At low frequencies, the impedance of the capacitor, C, is high. Therefore, the gain of the integrator is high. DC voltage at the output of the AD8236 is inverted and gained by the integrator. The inverted signal is injected back into the REF pin, nulling the output. In contrast, at high frequencies, the integrator has low gain because the impedance of C is low. Voltage changes at high frequencies are inverted but at a low gain. The signal is injected into the REF pins, but it is not enough to null the output. At very high frequencies, the capacitor appears as a short. The op amp is at unity gain. High frequency signals are, therefore, allowed to pass.

When a signal exceeds $f_{HIGH\text{-}PASS}$, the AD8236 outputs the high-pass filtered input signal.

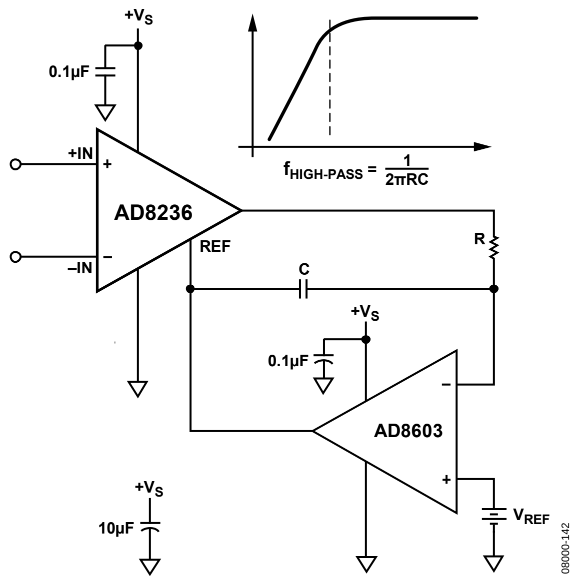


Figure 41. AC-Coupled Circuit

LOW POWER HEART RATE MONITOR

The low power and small size of the AD8236 make it an excellent choice for heart rate monitors. As shown in Figure 42, the AD8236 measures the biopotential signals from the body. It rejects common-mode signals and serves as the primary gain stage set at G = 5. The 4.7 μF capacitor and the 100 kΩ resistor set the −3 dB cutoff of the high-pass filter that follows the instrumentation amplifier. It rejects any differential dc offsets that may develop from the half-cell overpotential of the electrode.

A secondary gain stage, set at G = 403, amplifies the ECG signal, which is then sent into a second-order, low-pass, Bessel filter with −3 dB cutoff at 48 Hz. The 324 Ω resistor and 1 μF capacitor serve as an antialiasing filter. The 1 μF capacitor also serves as a charge reservoir for the ADC's switched capacitor input stage.

This circuit was designed and tested using the AD8609, low power, quad op amp. The fourth op amp is configured as a Schmitt trigger to indicate if the right arm or left arm electrodes fall off the body. Used in conjunction with the 953 kΩ resistors at the inputs of the AD8236, the resistors pull the inputs apart when the electrodes fall off the body. The Schmitt trigger sends an active low signal to indicate a leads off condition.

The reference electrode (right leg) is set tied to ground. Likewise, the shield of the electrode cable is also tied to ground. Some portable heart rate monitors do not have a third electrode. In such cases, the negative input of the AD8236 can be tied to GND.

Note that this circuit is shown, solely, to demonstrate the capability of the AD8236. Additional effort must be made to ensure compliance with medical safety guidelines.

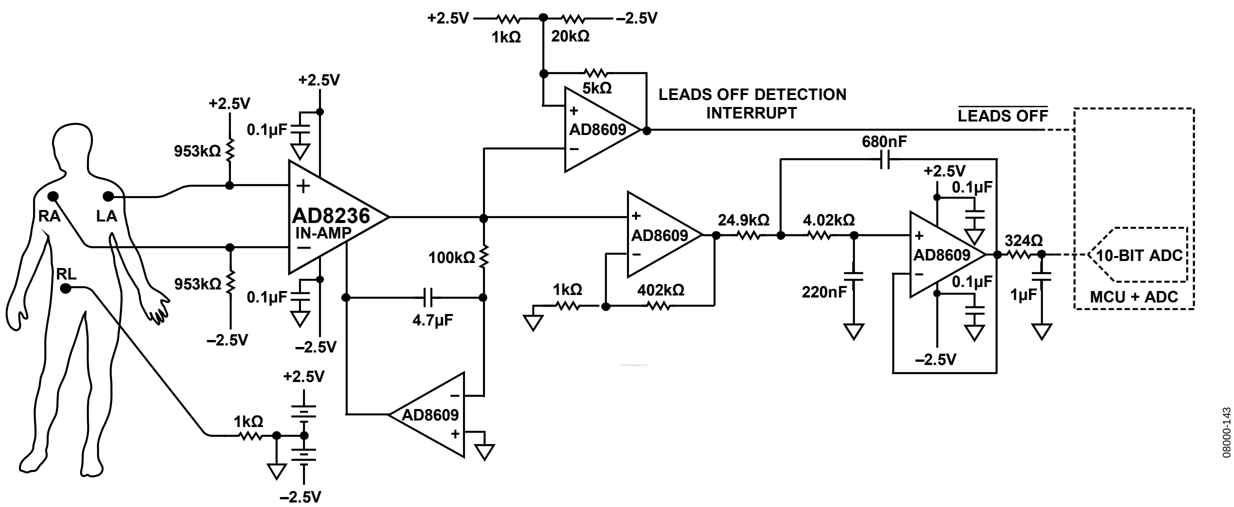


Figure 42. Example Low Power Heart Rate Monitor Schematic

OUTLINE DIMENSIONS

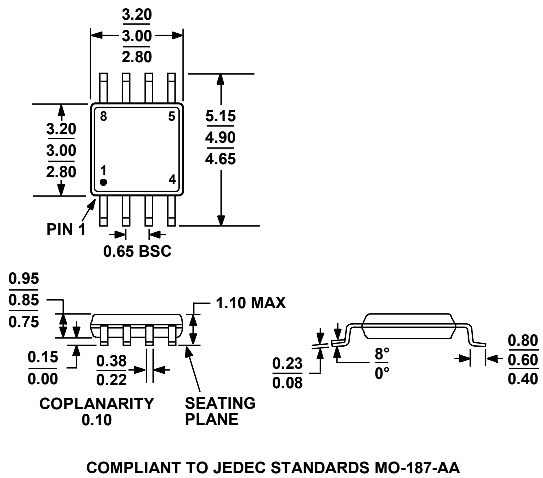


Figure 43. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding
AD8236ARMZ[1]	−40°C to +125°C	8-Lead MSOP	RM-8	Y1W
AD8236ARMZ-R7[1]	−40°C to +125°C	8-Lead MSOP	RM-8	Y1W
AD8236ARMZ-RL[1]	−40°C to +125°C	8-Lead MSOP	RM-8	Y1W

[1] Z = RoHS Compliant Part.

D08000-0-5/09(0)